I. Base du rapport

Le présent rapport d'examen préliminaire international se base sur la demande telle que déposée initialement.

V. Déclaration motivée selon la règle 66.2.a (ii) quant à la nouveauté, l'activité inventive et la possibilité d'application industrielle

A la lumière des documents cités dans le rapport de recherche internationale, il est considéré que l'invention telle que définie dans les revendications répond aux critères énoncés à l'article 33.1 PCT, c'est-à-dire qu'elle est nouvelle, qu'elle implique une activité inventive et qu'elle est susceptible d'application industrielle.

4. (currently amended) The communication interface according to Claim 1, wherein the DUT can operate at varying clock speeds and wherein the clock portion comprises:

a system clock line; and

a line for supplying an internal clock signal from the DUT to the emulator device;.

5. (original) A communication interface, comprising:

an interface;

a microcontroller;

an emulator device implemented a microcontroller and executing instructions;

wherein the microcontroller is coupled to the emulator device via the interface, the microcontroller executing the instructions in lock-step with the emulator device; and

wherein the interface comprises:

a first time dependent date line;

a second bi-directional time dependent data line;

a third line for supplying an internal clock signal from the microcontroller; and

a system clock line.

6. (original) The communication interface according to Claim 5, wherein the emulator device comprises a field programmable gate array (FPGA).

7. (original) The communication interface according to Claim 5, wherein the first time dependent data line is used to convey information regarding pending interrupts.

8. (original) The communication interface according to Claim 5, wherein the second bi-direction time dependent data line carries break signals.

9. (original) The communication interface according to Claim 5, wherein the interface lines are carried over a Category five cable.

10. (original) The communication interface according to Claim 5, wherein register read/write commands are conveyed over the first and second data lines when the microcontroller is in a halted mode.

11. (original) The communication interface according to Claim 5, wherein the first and second data lines are used to convey register information from the microcontroller to the emulator device when the microcontroller is in a halted mode.

12. (currently amended) The communication interface according to Claim 5, wherein the first and second data lines are used to communicated I/O read, interrupt vector and watchdog timer information when the microcontroller is running.

13. (original) The communication interface according to Claim 5, wherein commands and data for the microcontroller are communicated over the interface for programming flash memory forming a part of the microcontroller.

14. (original) The communication interface according to Claim 5, wherein the clock frequency of the microcontroller is programmable, and wherein the clock is supplied to the emulator devices over the third line of the interface.

15. (original) The communication interface according to Claim 5, wherein the microcontroller transfers I/O data over the interface at a rate adequate to permit the emulator device to process the I/O data before execution of a next instruction and thus keep the microcontroller and the emulation device in synchronization.

16. (original) The communication interface according to Claim 5, wherein the microcontroller uses the interface to return register information when in a halted mode, and to send I/O read, interrupt vector, and watchdog information when not in a halted mode.

17. (original) A four-wire interface for use in an in-circuit emulation (ICE) system to couple a microcontroller with an emulator device functioning as a virtual microcontroller, comprising:

a first interface line carrying a system clock driven by the microcontroller, for driving the communication state machines forming a part of the virtual microcontroller;

a second interface line carrying an internal microcontroller CPU clock;

a third interface line for use by the microcontroller to send I/O data to the ICE and to notify the ICE of pending interrupts; and

a fourth interface line for bi-directional communication that is used by the microcontroller to send I/O data to the ICE, and that is used by the ICE to convey halt requests to the microcontroller.

18. (original) The apparatus according to Claim 17, wherein the system clock runs at a first clock rate, unless the internal microcontroller CPU clock is running at the first clock rate in which case the system clock switches to two times the first clock rate.

19. (original) The apparatus according to Claim 17, wherein the interface lines are carried over a Category five cable.

20. (original) The apparatus according to Claim 17, wherein register read/write commands are conveyed over the third and fourth interface lines when the microcontroller is in a halted mode.

21. (original) The apparatus according to Claim 17, wherein the third and fourth interface lines are used to convey register information from the

microcontroller to the emulator device when the microcontroller is in a halted mode.

22. (currently amended) The apparatus according to Claim 17, wherein the third and fourth interface lines are used to communicated I/O read, interrupt vector and watchdog timer information when the microcontroller is running.

23. (original) The apparatus according to Claim 17, wherein commands and data for the microcontroller are communicated over the third and fourth interface lines for programming flash memory forming a part of the microcontroller.

24. (original) The apparatus according to Claim 17, wherein test and control functions are carried over the third and fourth interface lines to carry out real-time trace functions.

25. (original) The apparatus according to Claim 17, wherein the microcontroller sends I/O data over the interface at a rate adequate to keep the microcontroller and the emulation device in synchronization.

26. (original) A four wire interface for use in an in-circuit emulation (ICE) system to couple a microcontroller with an emulator device based on a field programmable gate array (FPGA) functioning as a virtual microcontroller, comprising:

a first interface line carrying a system clock driven by the microcontroller, for driving the communication state machines forming a part of the virtual microcontroller;

a second interface line carrying an internal microcontroller CPU clock, where in the clock frequency of the microcontroller is programmable;

wherein the system clock runs at a first clock rate, unless the internal microcontroller CPU clock is running at the first clock rate in which case the system clock switches to two times the first clock rate;

a third interface line for use by the microcontroller to send I/O data to the ICE and to notify the ICE of pending interrupts;

a fourth interface line used for bi-directional communication that is used by the microcontroller to send I/O data to the ICE, and that is used by the ICE to convey halt requests to the microcontroller;

wherein register read/write commands are conveyed over the third and fourth interface lines when the microcontroller is in a halted mode and wherein the third and fourth interface lines are used to communicated I/O read, interrupt vector and watchdog timer information when the microcontroller is running;

wherein test and control functions are carried over the third and fourth interface lines to carry out real-time trace functions;

wherein the microcontroller sends I/O data over the interface at a rate adequate to keep the microcontroller and the emulation device in synchronization; and

wherein the interface lines are carried over a Category five cable.